REMARKS/ARGUMENTS

The foregoing amendment revises claims to clarify that a clock signal having a relatively high frequency is supplied to a vertical drive circuit and that a clock signal having relatively low frequency is supplied to both a timing control circuit and a horizontal drive circuit. Support for these amendments can be found throughout the specification and in the drawings. See, e.g., Figure 3. No new matter has been added.

Independent claims 1 and 4, and dependent claim 3, have been rejected under 35 USC 103(a) as being unpatentable over Ito (USP 5,513,103) in view of Suzuki (USP 4,686,571) and further in view of Watanabe (USP 5,731,833). Applicant respectfully traverses this rejection.

One feature of the claimed invention is using two reference clock signals (see e.g., MCK and DCK shown in Figure 3) having different frequencies to drive a solid-state imaging apparatus. A first reference clock signal (MCK) has a first frequency and a second reference clock signal (DCK) has a second frequency that is lower than the first frequency.

The first reference clock signal is used for generating a vertical transfer clock signal (φv), which is used for vertically transferring information charges from a light receiving portion to a storing portion. The second reference clock signal is used for generating a horizontal transfer clock signal (φh), a horizontal timing signal (HD), and a vertical timing signal (VD). In other words, the frequency of the second reference clock signal (DCK) used for generating the signals (φh, HD, VD) is lower than that of the vertical transfer clock signal (φv).

In particular, the first reference clock signal (e.g., MCK) is supplied to a vertical drive circuit (12), which generates the vertical transfer clock signal, while the second clock signal (DCK) is supplied to a horizontal drive circuit (13), which generates the horizontal transfer clock signal, and a timing control circuit (14), which generates the horizontal timing signal and the vertical timing signal. Thus, it is unnecessary to vary the frequency of the first clock signal even if there is a need to vary the frequency of the second reference clock signal. This enables high-speed vertical transferring of information charges in any situation without being

influenced by frequency variation of the horizontal transfer clock signal and/or the timing signals. As a result, smearing can be significantly reduced.

Fig. 5 of Suzuki (US 4,686,571) shows two frequency dividers 51 and 52 for generating two clock signals having different frequencies f1 and f2 (f1>f2). An OR gate circuit 57 selects one of the two clock signals f1 and f2. The selected clock signal is supplied to an image unit 2, a storage unit 3 and a read-out register 4 (see Fig. 3). However, Suzuki does not suggest simultaneously providing the image unit 2, the storage unit 3 and the read-out register 4 with clock signals having different frequencies. In particular, Suzuki does not suggest providing the image unit with a reference clock signal having relatively high frequency f1 while providing the storage unit and the read-out register with a clock signal having relatively low frequency f2. Furthermore, Suzuki does not disclose the use of timing pulses for horizontal/vertical scanning.

In addition, as acknowledged by the Examiner, neither Ito (US 5,515,103) nor Watanabe (US 5,731,833) disclose this feature. As described at Col.6, lines 17-36 of Ito (US 5,515,103), a timing control circuit 19 generates timing pulses for horizontal/vertical scanning of a CCD device based on a reference clock signal. (Note that the timing pulses for horizontal/vertical scanning correspond to the horizontal timing signal HD and the vertical timing signal VD of the claimed invention, respectively.). However, there is no description regarding the frequency of the reference clock signal. Ito suggests neither that two reference clock signals having different frequencies are used to generate clock signals for driving a solid-state imaging apparatus nor that timing pulses for horizontal/vertical scanning are generated based on a reference clock signal having a relatively low frequency. Furthermore, Ito does not disclose generating transfer clock signals corresponding to the horizontal and vertical transfer clock signals (φh, φv) of the claimed invention.

Watanabe (US 5,731,833) simply discloses generating a horizontal timing signal HT and a vertical timing signal VT from a constant reference clock CK. However, Watanabe does not suggest providing an image unit with a reference clock signal having relatively high

frequency while providing a storage unit and a read-out register with a clock signal having relatively low frequency.

Thus, none of Suzuki, Ito and Watanabe suggest of providing the image unit with a reference clock signal having a relatively high frequency and providing the storage unit and the read-out register with a clock signal having relatively low frequency. Thus, Applicants respectfully request that the Examiner reconsider and withdraw the rejection in light of the amendments and arguments made herein, and that claims 1, 2 and 4 be allowed.

The Examiner also rejected claims 1, 2 and 4 under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art in view of Suzuki (4,686,571). Applicant respectfully traverses this rejection.

As admitted by the Examiner, Applicants' admitted prior art "fails to specifically disclose that the vertical drive circuit generates a vertical drive circuit [that] generates a vertical transfer clock from a second clock, which is shorter than the first clock, or that the horizontal transfer [circuit] generates a horizontal transfer clock from the first clock." As described above, Suzuki also fails to disclose the requirement of the claims as amended of providing the image unit with a reference clock signal having a relatively high frequency and providing the storage unit and the read-out register with a clock signal having relatively low frequency. Thus, Applicants respectfully request that the Examiner reconsider and withdraw the rejection of claims 1, 2 and 4 in light of the amendments and arguments made herein, and that claims 1, 2 and 4 be allowed.

CONCLUSION

Based upon the foregoing, Applicants believe that all pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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Amended sheet #1

Fig.1 (Prior Art)

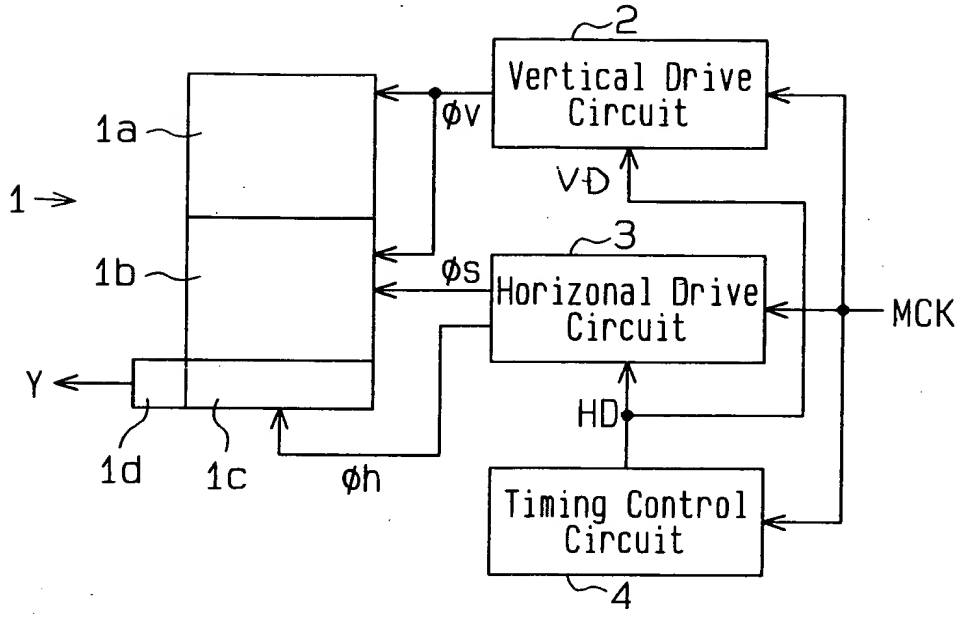
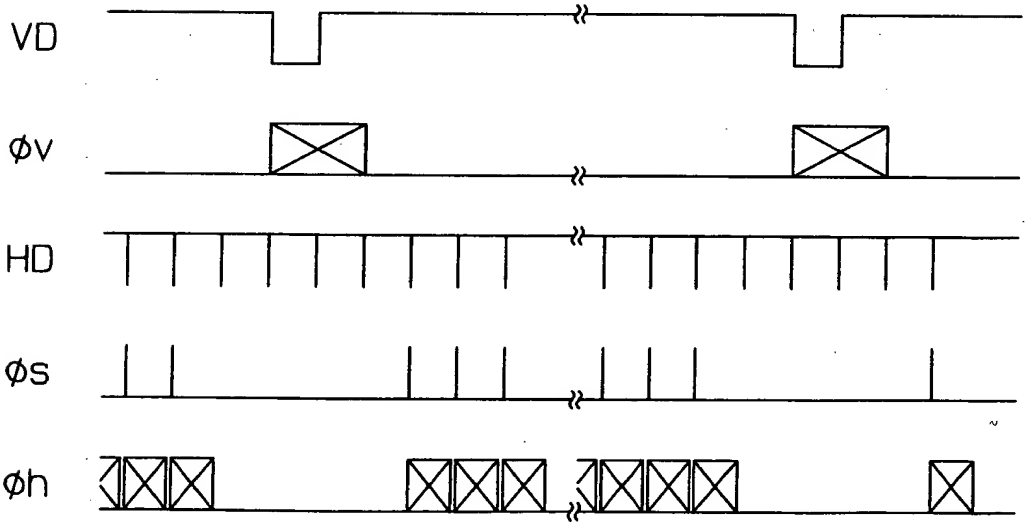


Fig.2 (Prior Art)



Amended sheet #2

Fig.3

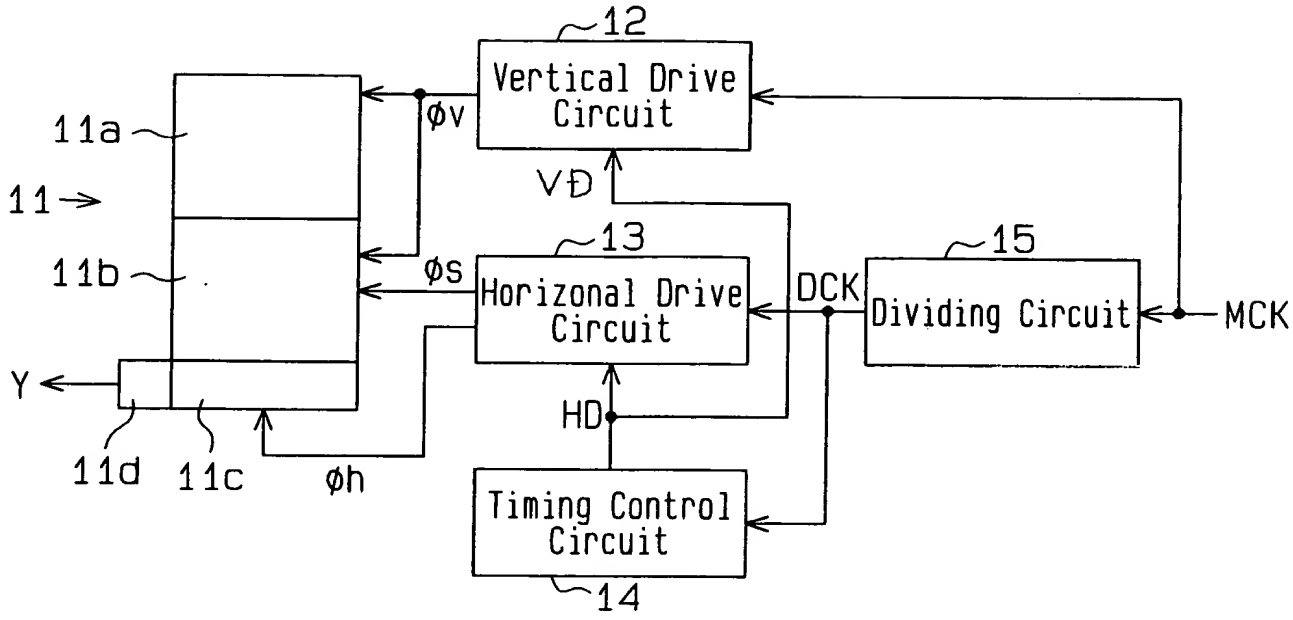


Fig.4